

### Features

- Single power supply voltage of 3.0V to 3.6V
- Power down features using CE1# and CE2
- Low power dissipation
- Data retention supply voltage: 1.5V to 3.6V
- Direct TTL compatibility for all input and output
- Wide operating temperature range: -40°C to 85°C
- Standby current @ VDD = 3.6 V

### Ordering Information

Part Number	Speed	I <sub>DD2</sub>	Package
EM564161BC-55	55 ns	35 $\mu$ A	6x8 BGA
EM564161BC-70	70 ns	35 $\mu$ A	6x8 BGA
EM564161BC-85	85 ns	35 $\mu$ A	6x8 BGA

### Pin Description

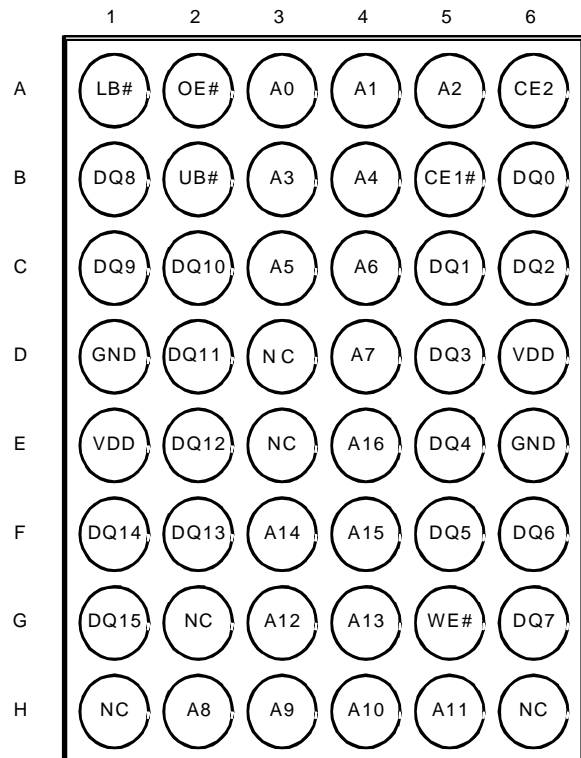
Symbol	Function
A0 - A17	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
CE1#, CE2	Chip Enable Inputs
OE#	Output Enable
WE#	Read / Write Control Input
LB#, UB#	Data Byte Control Inputs
GND	Ground
VDD	Power Supply
NC	No Connection

### Overview

The EM564161 is a 4,194,304-bit SRAM organized as 262,144 words by 16 bits. It is designed with advanced CMOS technology. This Device operates from a single 3.0V to 3.6V power supply. Advanced circuit technology provides both high speed and low power. It is automatically placed in low-power mode when chip enable (CE1#) is asserted high or (CE2) is asserted low. There are three control inputs. CE1# and CE2 are used to select the device and for data retention control, and output enable (OE#) provides fast memory access. Data byte control pin (LB#,UB#) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range from -40°C to 85°C, the EM564161 can be used in environments exhibiting extreme temperature conditions.

### Pin Configuration

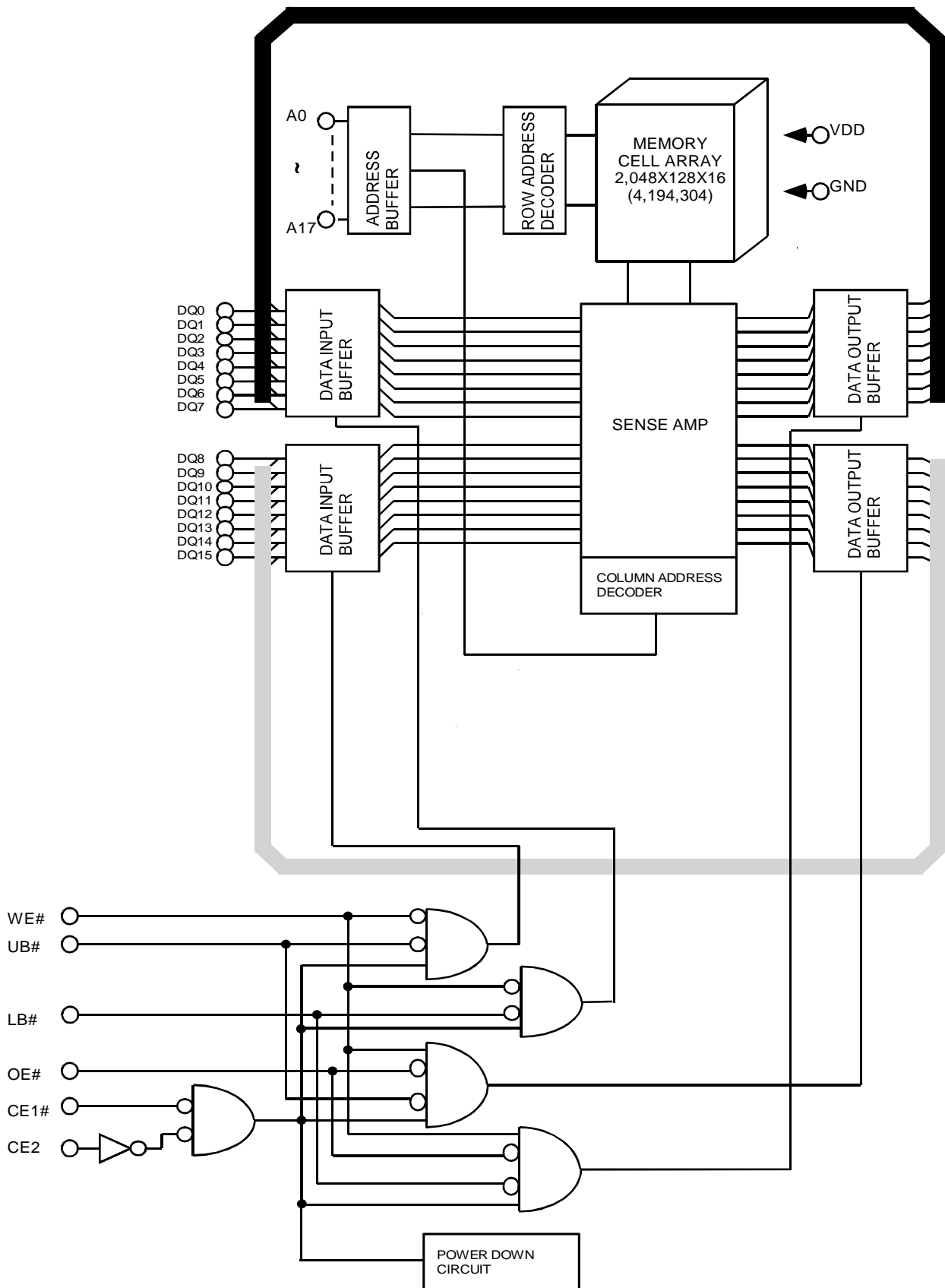
48-Ball BGA Top View



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## Block Diagram



## Operating Mode

Mode	CE1#	CE2	OE#	WE#	LB#	UB#	DQ0~DQ7	DQ8~DQ15
Read	L	H	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>
					H	L	High-Z	D <sub>OUT</sub>
					L	H	D <sub>OUT</sub>	High-Z
Write	L	H	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>
					H	L	High-Z	D <sub>IN</sub>
					L	H	D <sub>IN</sub>	High-Z
Output Deselect	L	H	H	H	X	X	High-Z	High-Z
	L	H	X	X	H	H		
Standby	H	X	X	X	X	X	High-Z	High-Z
	X	L	X	X	X	X		

Note: X = don't care. H=logic high. L=logic low.

## Absolute Maximum Ratings

Supply voltage, V <sub>DD</sub>	-0.3 to +4.6V
Input voltages, V <sub>IN</sub>	-0.3 to +4.6V
Input and output voltages, V <sub>I/O</sub>	-0.5 to V <sub>DD</sub> +0.5V
Operating temperature, T <sub>OPR</sub>	-40 to +85°C
Storage temperature, T <sub>STRG</sub>	-55 to +150°C
Soldering Temperature (10s), T <sub>SOLDER</sub>	240°C
Power dissipation, P <sub>D</sub>	0.6 W

## DC Recommended Operating Conditions (Ta=-40°C to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>DD</sub>	Power Supply Voltage	3.0	–	3.6	V
V <sub>IH</sub>	Input High Voltage	2.7	–	V <sub>DD</sub> + 0.3 <sup>(1)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(2)</sup>	–	0.6	V
V <sub>DR</sub>	Data Retention Supply Voltage	1.5	–	3.6	V
I <sub>DR</sub>	Data Retention Supply Current	–	–	35	μA

Note:

(1) Overshoot : V<sub>DD</sub> +2.0V in case of pulse width ≤ 20ns

(2) Undershoot : -2.0V in case of pulse width ≤ 20ns

## DC Characteristics (Ta = -40°C to 85°C, V<sub>DD</sub> = 3.0V to 3.6V)

Parameter	Symbol	Test Conditions		Min	Max	Unit	
Input low current	I <sub>IL</sub>	I <sub>IN</sub> = 0V to V <sub>DD</sub>		- 1	1	μA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA		-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA		V <sub>DD</sub> - 0.15	-	V	
Operating current	I <sub>DD1</sub>	CE1# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> and I <sub>OUT</sub> = 0mA Other Input = V <sub>IH</sub> / V <sub>IL</sub>	Cycle time = min 55	V <sub>DD</sub> = 3.6 V	-	35	mA
			70/85	V <sub>DD</sub> = 3.6 V	-	25	
	I <sub>DD2</sub>	Cycle time = 1μs		-	5		
Standby current	I <sub>DD2</sub> * (Note)	CE1# = V <sub>DD</sub> - 0.2V or CE2 = 0.2V	55/70/85	V <sub>DD</sub> = 3.6 V	-	35	μA

### Notes:

\* In standby mode with CE1# ≥ V<sub>DD</sub> - 0.2V, these limits are assured for the condition CE2 ≥ V<sub>DD</sub> - 0.2V or CE2 ≤ 0.2V.

## Capacitance (Ta = 25°C; f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C <sub>IN</sub>	-	-	10	pF	V <sub>IN</sub> = GND
Output capacitance	C <sub>OUT</sub>	-	-	10	pF	V <sub>OUT</sub> = GND

**Notes:** This parameter is periodically sampled and is not 100% tested.

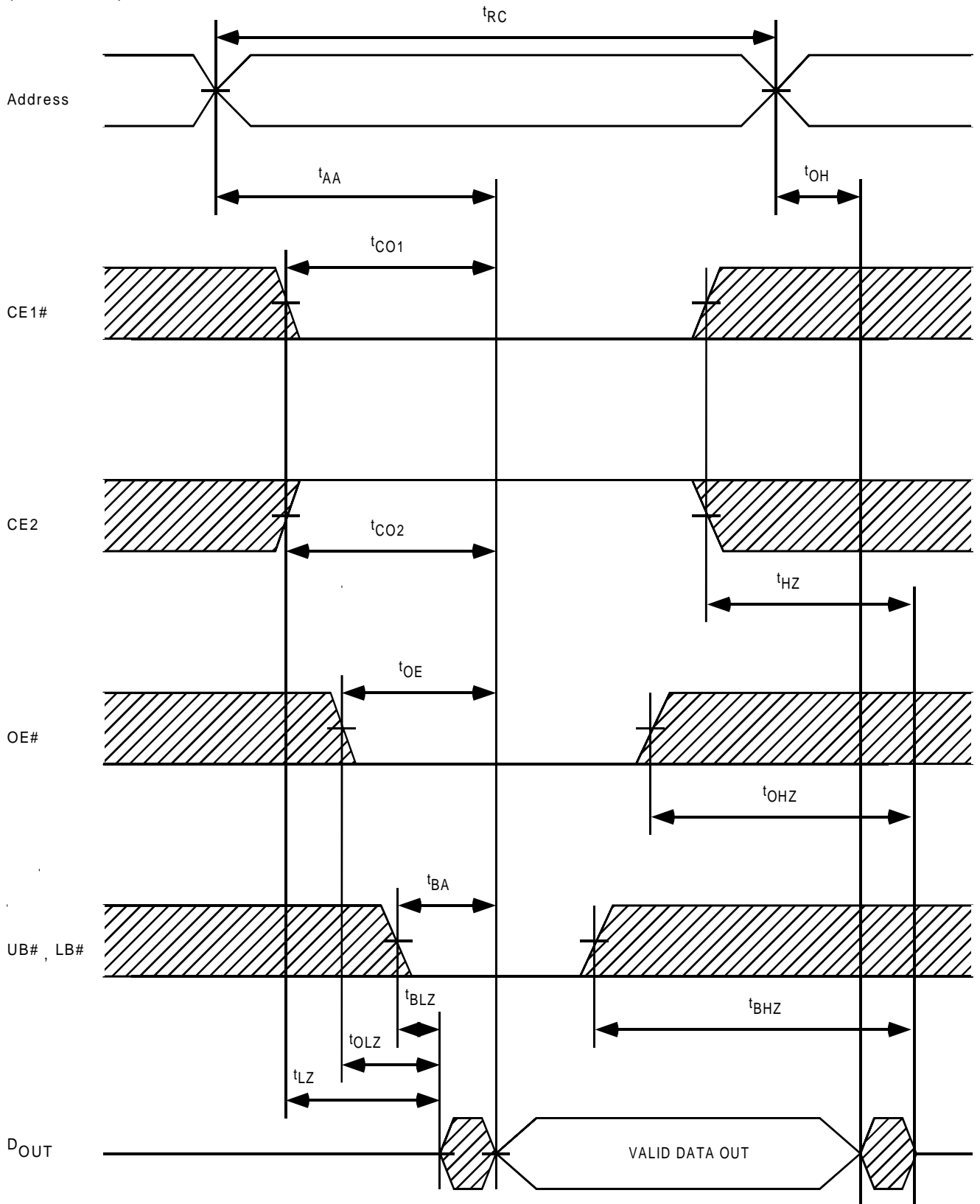
## AC Characteristics and Operating Conditions (Ta = -40°C to 85°C, VDD = 3.0V to 3.6V)

Read Cycle								
Symbol	Parameter	EM564161						Unit
		-55		-70		-85		
		Min	Max	Min	Max	Min	Max	
t <sub>RC</sub>	Read cycle time	55	–	70	–	85	–	ns
t <sub>AA</sub>	Address access time	–	55	–	70	–	85	
t <sub>CO1</sub>	Chip Enable (CE1#) Access Time	–	55	–	70	–	85	
t <sub>CO2</sub>	Chip Enable (CE2) Access Time	–	55	–	70	–	85	
t <sub>OE</sub>	Output enable access time	–	25	–	35	–	45	
t <sub>BA</sub>	Data Byte Control Access Time	–	55	–	70	–	85	
t <sub>LZ</sub>	Chip Enable Low to Output in Low-Z	10	–	10	–	10	–	
t <sub>OLZ</sub>	Output enable Low to Output in Low-Z	3	–	3	–	3	–	
t <sub>BLZ</sub>	Data Byte Control Low to Output in Low-Z	5	–	5	–	5	–	
t <sub>HZ</sub>	Chip Enable High to Output in High-Z	–	20	–	25	–	35	
t <sub>OHZ</sub>	Output Enable High to Output in High-Z	–	20	–	25	–	35	
t <sub>BHZ</sub>	Data Byte Control High to Output in High-Z	–	20	–	25	–	35	
t <sub>OH</sub>	Output Data Hold Time	0	–	0	–	0	–	
Write Cycle								
Symbol	Parameter	EM564161						Unit
		-55		-70		-85		
		Min	Max	Min	Max	Min	Max	
t <sub>WC</sub>	Write cycle time	55	–	70	–	85	–	ns
t <sub>WP</sub>	Write pulse width	45	–	55	–	55	–	
t <sub>CW</sub>	Chip Enable to end of write	45	–	60	–	70	–	
t <sub>BW</sub>	Data Byte Control to end of Write	45	–	60	–	70	–	
t <sub>AS</sub>	Address setup time	0	–	0	–	0	–	
t <sub>WR</sub>	Write Recovery time	0	–	0	–	0	–	
t <sub>WHZ</sub>	WE# Low to Output in High-Z	–	25	–	30	–	35	
t <sub>OW</sub>	WE# High to Output in Low-Z	5	–	5	–	5	–	
t <sub>DS</sub>	Data Setup Time	25	–	30	–	35	–	
t <sub>DH</sub>	Data Hold Time	0	–	0	–	0	–	

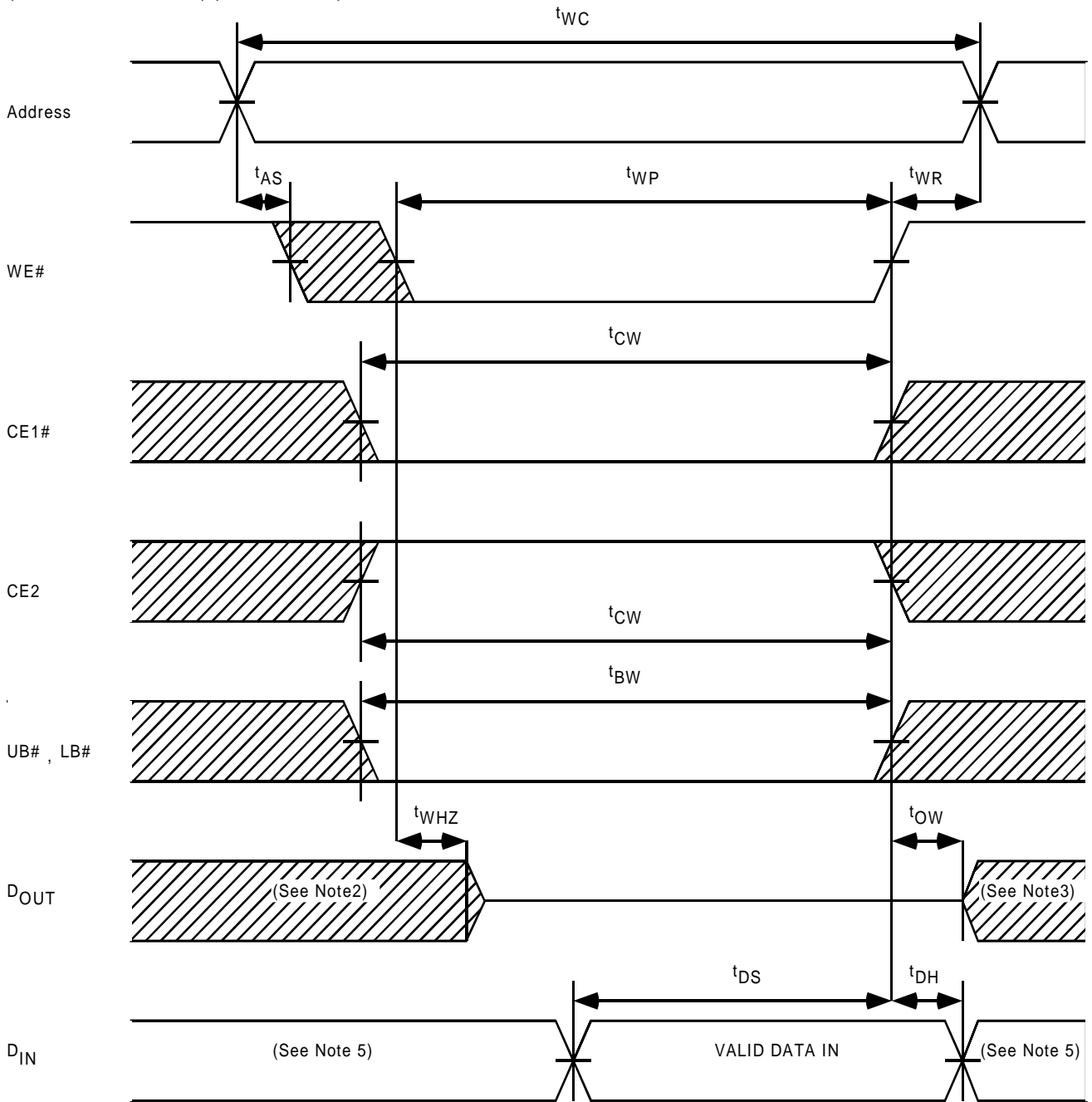
### AC Test Condition

- Output load : 50pF + one TTL gate
- Input pulse level : 0.4V, 2.4V
- Timing measurements : 0.5 x VDD
- tR, tF : 5ns

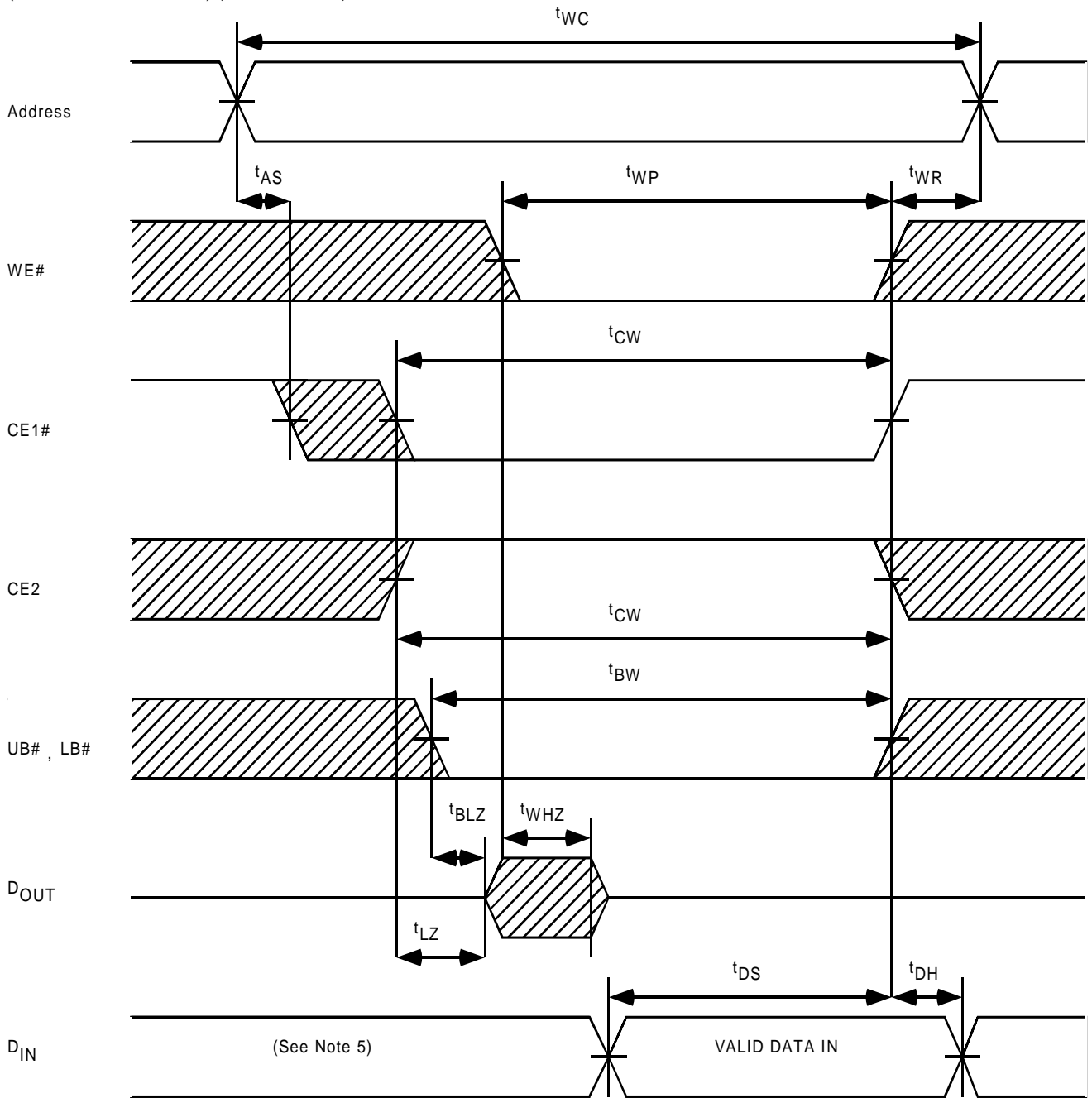
**Read Cycle**  
(See Note 1)



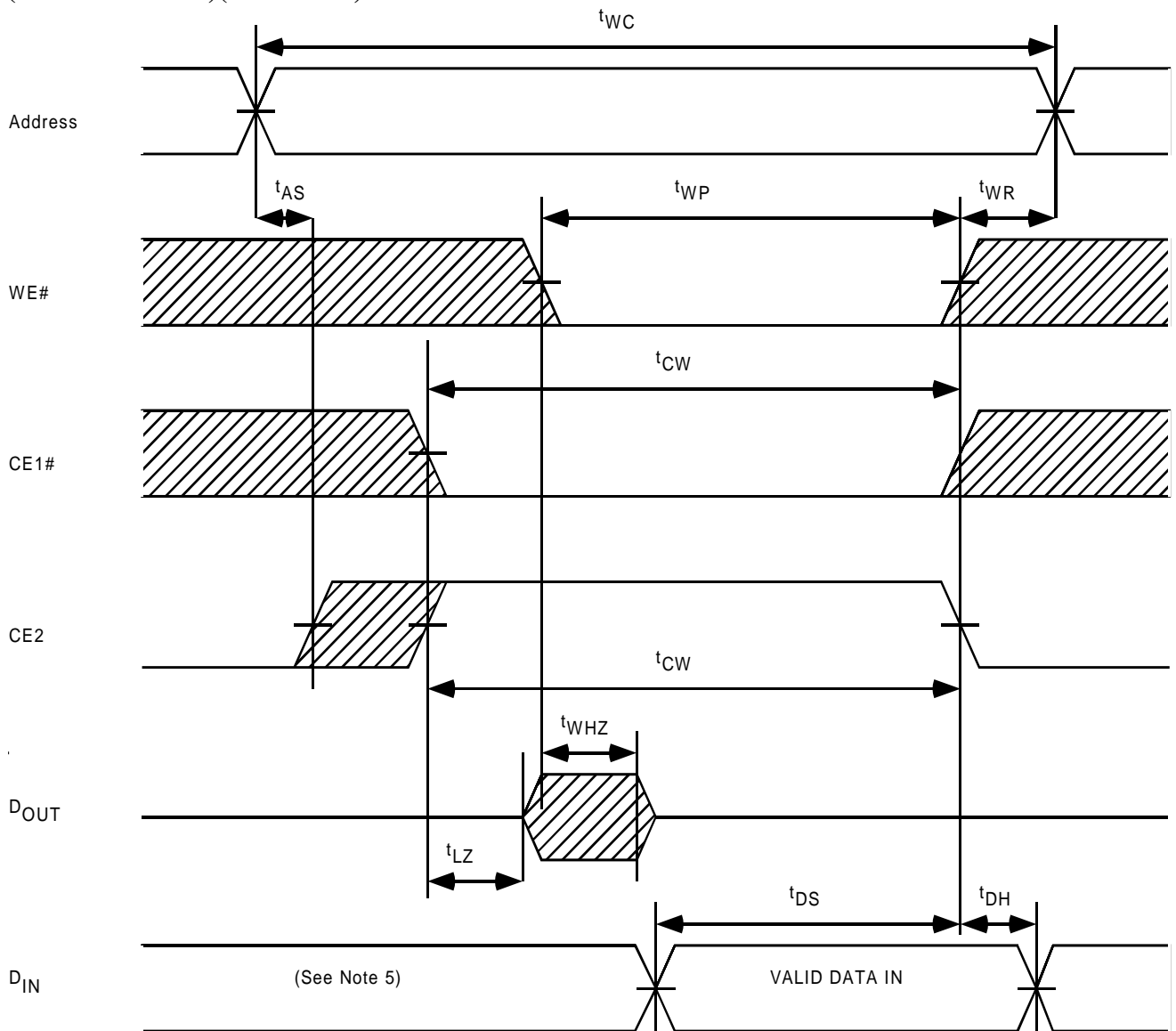
**Write Cycle1**  
**(WE# Controlled)(See Note 4)**



**Write Cycle 2**  
**(CE1# Controlled)(See Note 4)**

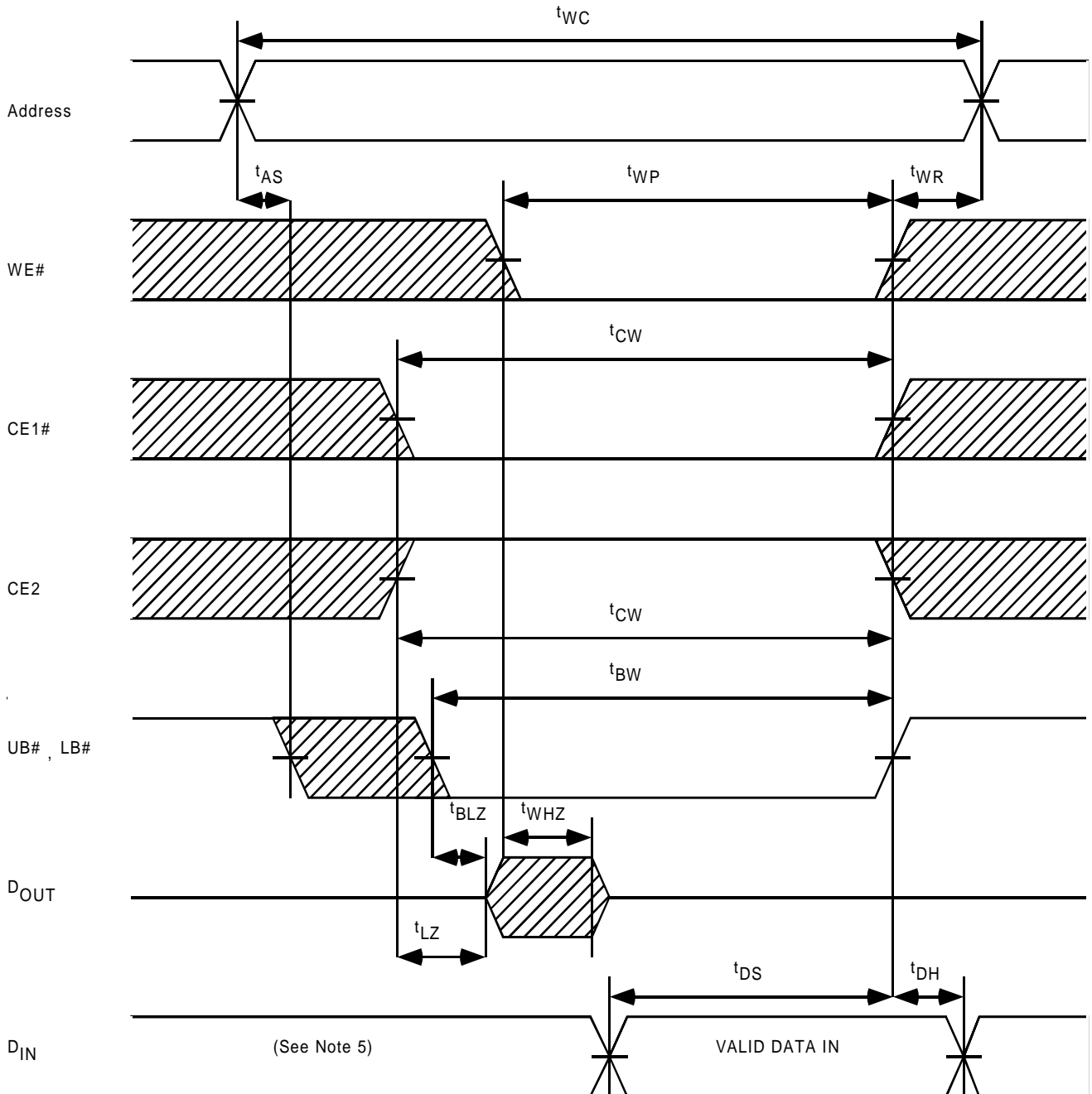


**Write Cycle 3**  
**(CE2 Controlled)(See Note 4)**



## Write Cycle4

(UB#, LB# Controlled)(See Note 4)



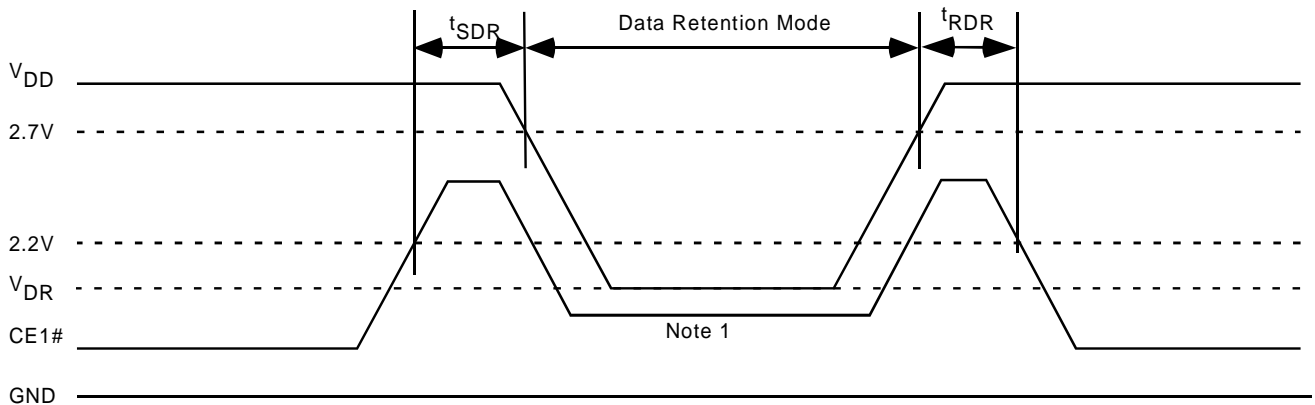
### Note:

1. WE# remains HIGH for the read cycle.
2. If CE1# goes LOW (or CE2 goes HIGH) with or after WE# goes LOW, the outputs will remain at high impedance.
3. If CE1# goes HIGH (or CE2 goes LOW) coincident with or before WE# goes HIGH, the outputs will remain at high impedance.
4. If OE# is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

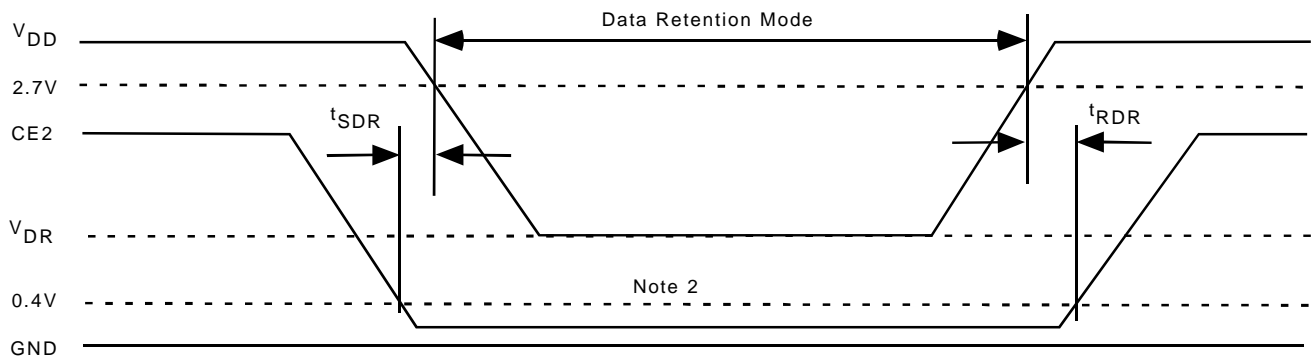
## Data Retention Characteristics (Ta = -40°C to 85°C)

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>DR</sub>	Data Retention Supply Voltage	CE1# ≥ V <sub>DD</sub> - 0.2V, CE2 ≤ 0.2V, VIN ≥ V <sub>DD</sub> - 0.2V or VIN ≤ 0.2V	1.5	–	3.6	V
I <sub>DR</sub>	Data Retention Supply Current	CE1# ≥ V <sub>DD</sub> - 0.2V, CE2 ≤ 0.2V, VIN ≥ V <sub>DD</sub> - 0.2V or VIN ≤ 0.2V	–	–	35	μA
t <sub>SDR</sub>	Chip Deselect to Data Retention Mode Time		0	–	–	ns
t <sub>RDR</sub>	Recovery Time		t <sub>RC</sub>	–	–	ns

### CE1# Controlled Data Retention Mode



### CE2 Controlled Data Retention Mode



### Note:

1. CE1# ≥ V<sub>DD</sub> - 0.2V or UB# = LB# ≥ V<sub>DD</sub> - 0.2V
2. CE2 ≤ 0.2V

## Package Diagrams

### 48-Ball (6mm x 8mm) BGA

Units in mm

TOP VIEW

BOTTOM VIEW

