

## 512K x 16 Low Power SRAM

Preliminary, Rev 1.2 Dec/2007

### Features

- Single Power Supply Voltage, 3.0 ~ 3.6 V
- Power Down Features Using CE1#, CE2, LB# and UB#
- Low Power Dissipation
- Data retention Supply Voltage: 1.5V to 3.6V
- Direct TTL Compatibility for All Input and Output
- Wide Operating Temperature Range: -40°C to 85°C
- Standby current (maximum) @ VDD = 3.6 V
- Lead Free Package available

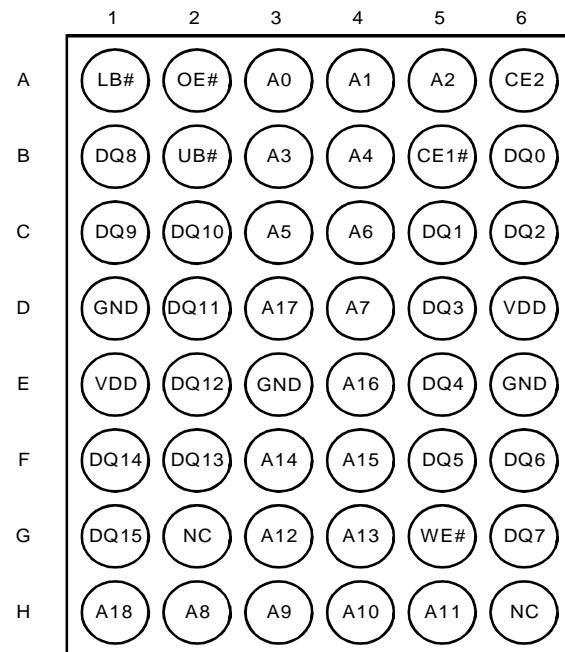
### Ordering Information

Part Number	Spee	IDDS2	Package
EM565161BJ-70/-70G	70 ns	35 $\mu$ A	6x9 BGA
EM565161BA-70/-70G	70 ns	35 $\mu$ A	8x10 BGA
EM565161BJ-55/-55G	55 ns	35 $\mu$ A	6x9 BGA
EM565161BA-55/-55G	55 ns	35 $\mu$ A	8x10 BGA

G : indicates Lead Free Package

### Pin Assignment

#### 48-Ball BGA (CSP), Top View



### Pin Names

Symbol	Function
A0 – A18	Address Inputs
DQ0-DQ15	Data Inputs/Outputs
CE1#,CE2	Chip Enable Input
OE#	Output Enable
WE#	Read/Write Control Input
LB#,UB#	Data Byte Control Inputs
GND	Ground
VDD	Power Supply
NC	No Connection

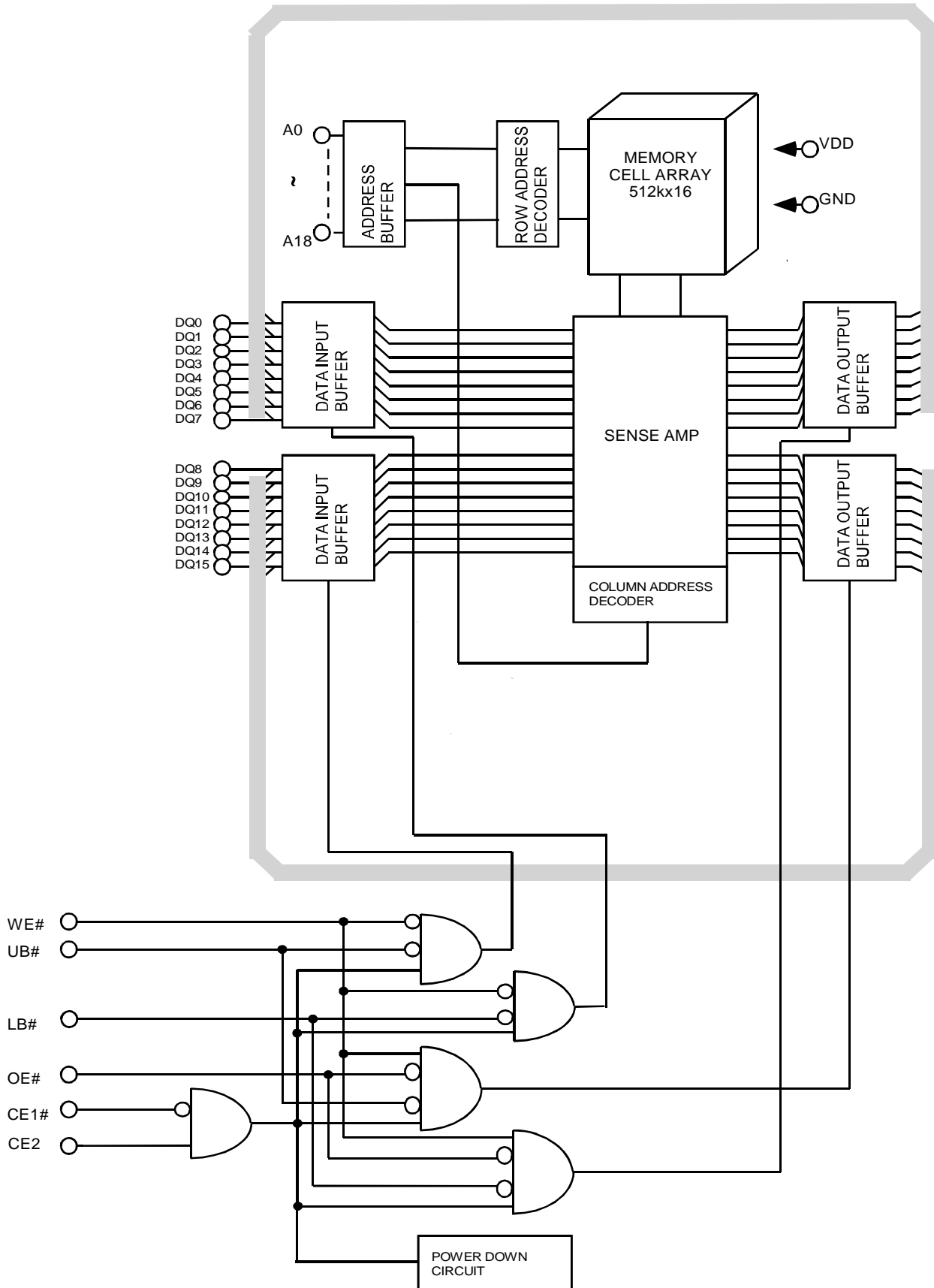
### Overview

The EM565161 is an 8M-bit SRAM organized as 512K words by 16 bits. It is designed with advanced CMOS technology. This Device operates from a single power supply. Advanced circuit technology provides both high speed and low power. It is automatically placed in low-power mode when CE1# or both UB# and LB# are asserted high or CE2 is asserted low. There are three control inputs. CE1# and CE2 are used to select the device and for data retention control, and output enable (OE#) provides fast memory access. Data byte control pin (LB#,UB#) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range from -40°C to 85°C, the EM565161 can be used in environments exhibiting extreme temperature conditions.

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## Block Diagram



## Operating Mode

Mode	CE1#	CE2	OE#	WE#	LB#	UB#	DQ0~DQ7	DQ8~DQ15	Power
Read	L	H	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>DDO</sub>
					H	L	High-Z	D <sub>OUT</sub>	I <sub>DDO</sub>
					L	H	D <sub>OUT</sub>	High-Z	I <sub>DDO</sub>
Write	L	H	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>DDO</sub>
					H	L	High-Z	D <sub>IN</sub>	I <sub>DDO</sub>
					L	H	D <sub>IN</sub>	High-Z	I <sub>DDO</sub>
Output Disabled	L	H	H	H	X	X	High-Z	High-Z	I <sub>DDO</sub>
	L	H	X	X	H	H	High-Z	High-Z	I <sub>DDO</sub>
Standby	H	X	X	X	X	X	High-Z	High-Z	I <sub>DDS</sub>
	X	L	X	X	X	X			
	X	X	X	X	H	H			

Note: X=don't care. H=logic high. L=logic low.

## Absolute Maximum Ratings

Supply voltage, V <sub>DD</sub>	-0.3 to +4.6V
Input voltages, V <sub>IN</sub>	-0.3 to +4.6V
Input and output voltages, V <sub>I/O</sub>	-0.5 to V <sub>DD</sub> +0.5V
Operating temperature, T <sub>OPR</sub>	-40 to +85°C
Storage temperature, T <sub>STRG</sub>	-55 to +150°C
Soldering Temperature (10s), T <sub>SOLDER</sub>	260°C
Power dissipation, P <sub>D</sub>	1 W

## DC Recommended Operating Conditions (Ta=-40°C to 85°C)

Symbol	Parameter	Min	Max	Unit
V <sub>DD</sub>	Power Supply Voltage	3.0	3.6	V
V <sub>IH</sub>	Input High Voltage	2.2	V <sub>DD</sub> + 0.3 <sup>(1)</sup>	
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(2)</sup>	0.6	
V <sub>DR</sub>	Data Retention Supply Voltage	1.0	3.6	

Note:

(1) Overshoot : V<sub>DD</sub> +2.0V in case of pulse width ≤ 20ns

(2) Undershoot : -2.0V in case of pulse width ≤ 20ns

## DC Characteristics (Ta = -40°C to 85°C, V<sub>DD</sub> = 3.0V to 3.6V)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input low current	I <sub>IL</sub>	I <sub>IN</sub> = 0V to V <sub>DD</sub>	- 1	1	μA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	V <sub>DD</sub> - 0.15	-	V	
Operating current	I <sub>DD1</sub>	CE1# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> and I <sub>OUT</sub> = 0mA Other Input = V <sub>IH</sub> / V <sub>IL</sub>	Cycle time = min	-	35	mA
	I <sub>DD2</sub>		Cycle time = 1μs	-	5	
Standby current	I <sub>DSS2</sub>	CE1# = V <sub>DD</sub> - 0.2V or UB# and LB# = V <sub>DD</sub> -0.2V or CE2 = 0.2V	-55	-	35	μA
			-70	-	35	

## Capacitance (Ta = 25°C; f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	C <sub>IN</sub>	-	8	pF	V <sub>IN</sub> = GND
Input/Output capacitance	C <sub>IO</sub>	-	10	pF	V <sub>IO</sub> = GND

**Notes:** This parameter is periodically sampled and is not 100% tested.

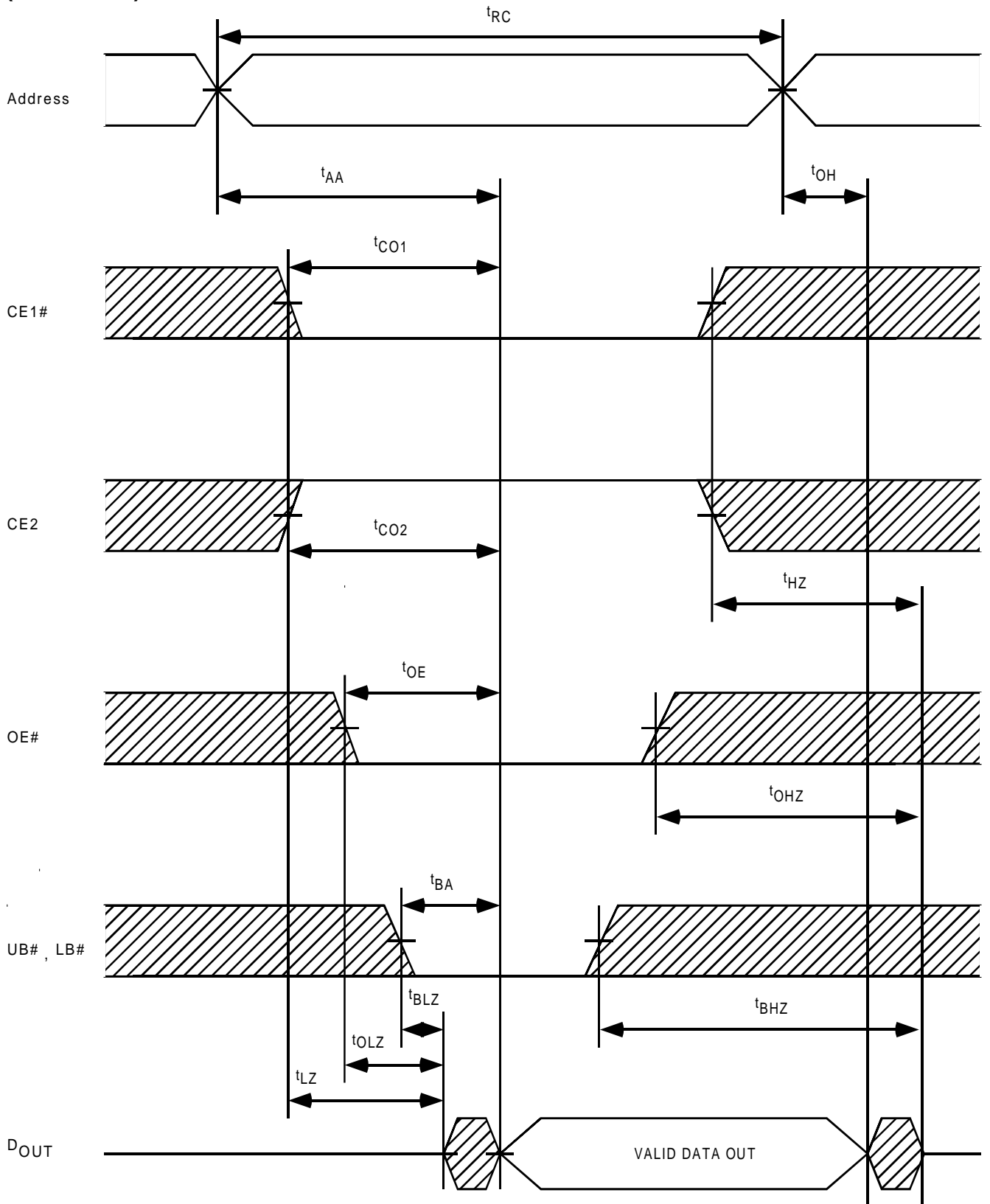
## AC Characteristics and Operating Conditions (Ta = -40°C to 85°C, VDD = 3.0V to 3.6V)

Read Cycle						
Symbol	Parameter	EM565161				Unit
		-55		-70		
		Min	Max	Min	Max	
t <sub>RC</sub>	Read cycle time	55	–	70	–	ns
t <sub>AA</sub>	Address access time	–	55	–	70	
t <sub>CO1</sub>	Chip Enable (CE1#) Access Time	–	55	–	70	
t <sub>CO2</sub>	Chip Enable (CE2) Access Time	–	55	–	70	
t <sub>OE</sub>	Output enable access time	–	25	–	35	
t <sub>BA</sub>	Data Byte Control Access Time	–	55	–	70	
t <sub>LZ</sub>	Chip Enable Low to Output in Low-Z	10	–	10	–	
t <sub>OLZ</sub>	Output enable Low to Output in Low-Z	5	–	5	–	
t <sub>BLZ</sub>	Data Byte Control Low to Output in Low-Z	10	–	10	–	
t <sub>HZ</sub>	Chip Enable High to Output in High-Z	–	20	–	25	
t <sub>OHZ</sub>	Output Enable High to Output in High-Z	–	20	–	25	
t <sub>BHZ</sub>	Data Byte Control High to Output in High-Z	–	20	–	25	
t <sub>OH</sub>	Output Data Hold Time	0	–	0	–	
Write Cycle						
Symbol	Parameter	EM565161				Unit
		-55		-70		
		Min	Max	Min	Max	
t <sub>WC</sub>	Write cycle time	55	–	70	–	ns
t <sub>WP</sub>	Write pulse width	45	–	55	–	
t <sub>CW</sub>	Chip Enable to end of write	45	–	60	–	
t <sub>BW</sub>	Data Byte Control to end of Write	45	–	60	–	
t <sub>AS</sub>	Address setup time	0	–	0	–	
t <sub>WR</sub>	Write Recovery time	0	–	0	–	
t <sub>WHZ</sub>	WE# Low to Output in High-Z	–	20	–	20	
t <sub>OW</sub>	WE# High to Output in Low-Z	5	–	5	–	
t <sub>DS</sub>	Data Setup Time	25	–	30	–	
t <sub>DH</sub>	Data Hold Time	0	–	0	–	

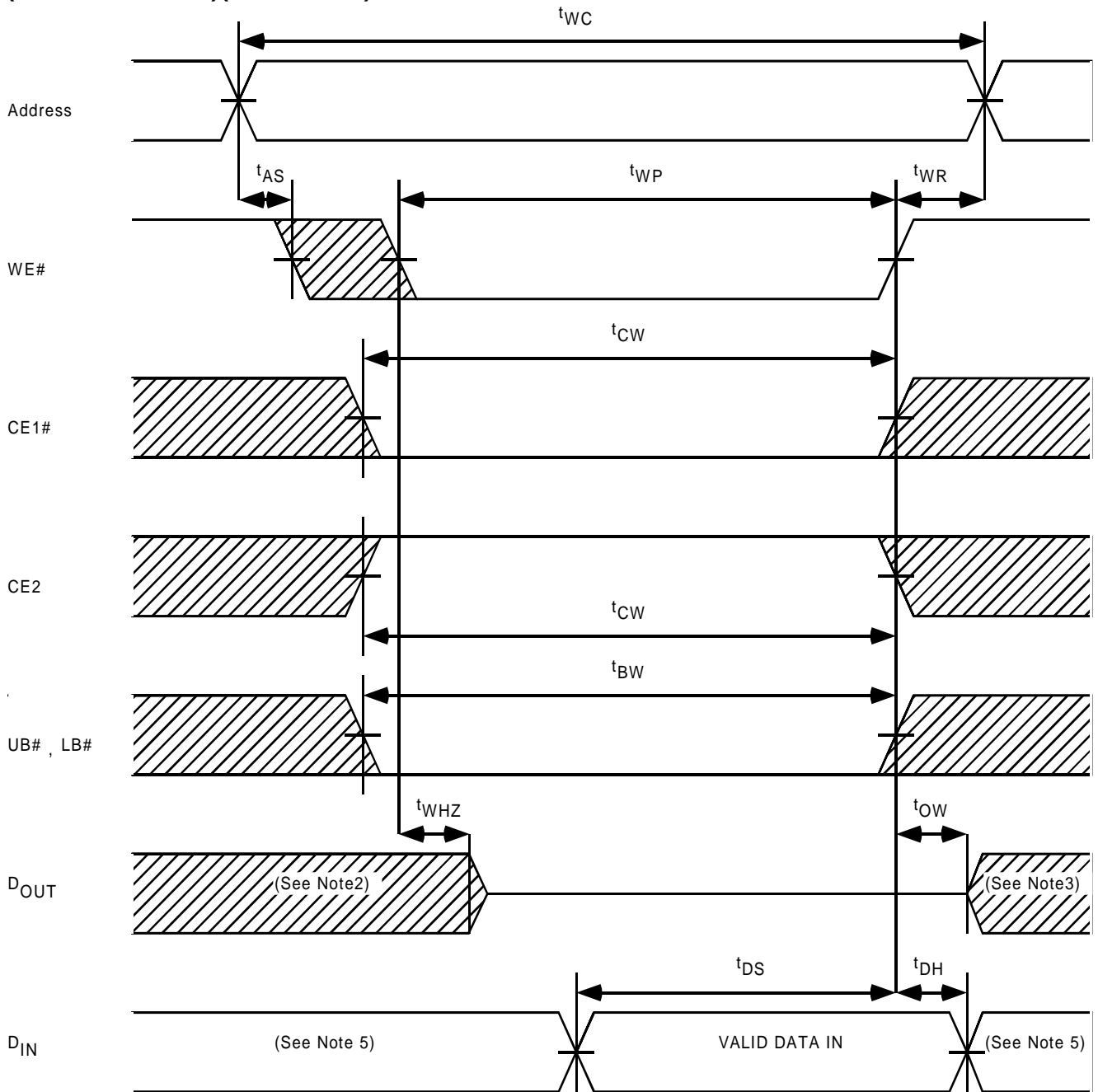
### AC Test Condition

- Output load : 60pF + one TTL gate
- Input pulse level : 0.4V, 2.4V
- Timing measurements : 0.5 x VDD
- t<sub>R</sub>, t<sub>F</sub> : 5ns

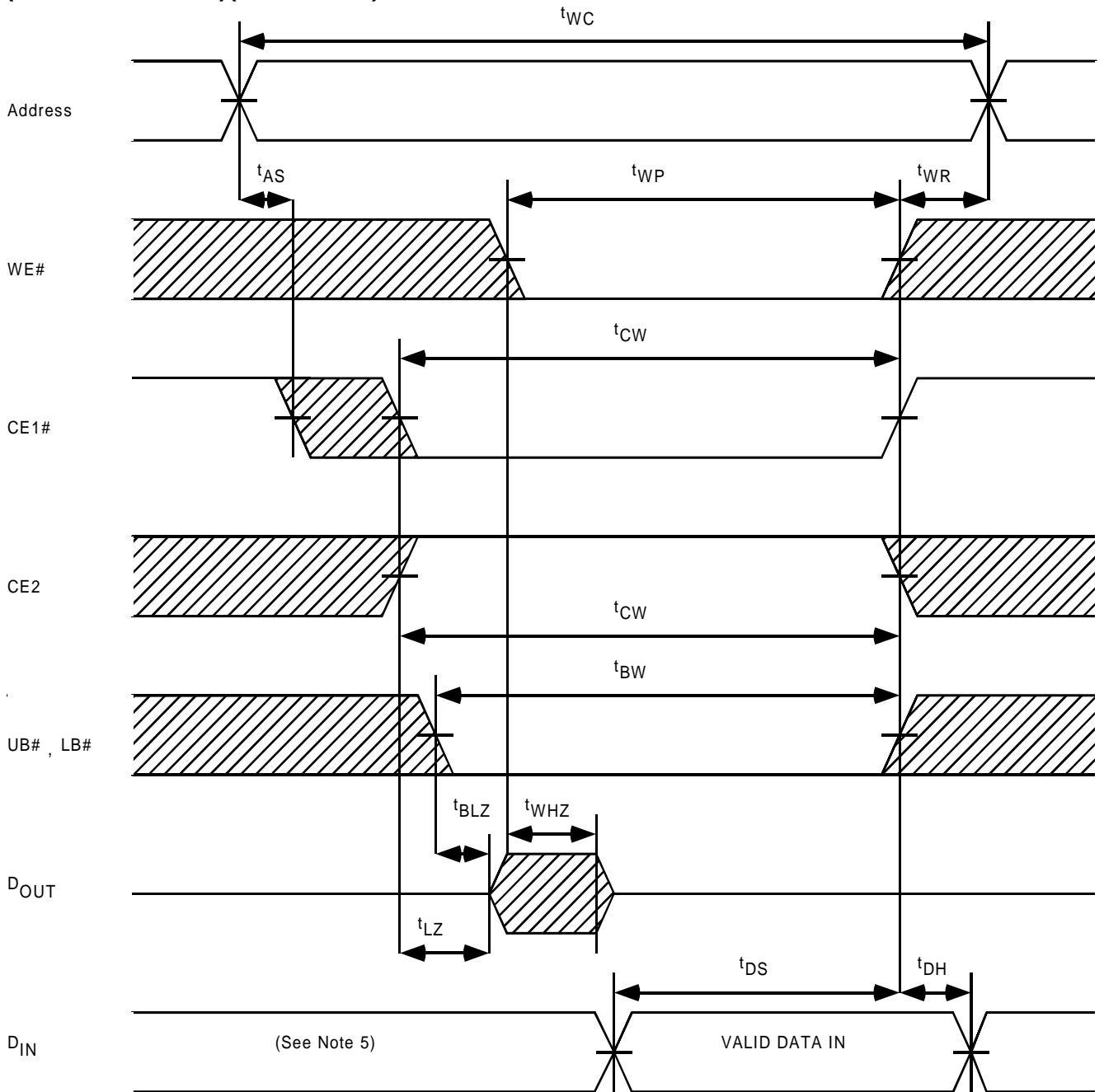
## Read Cycle (See Note 1)



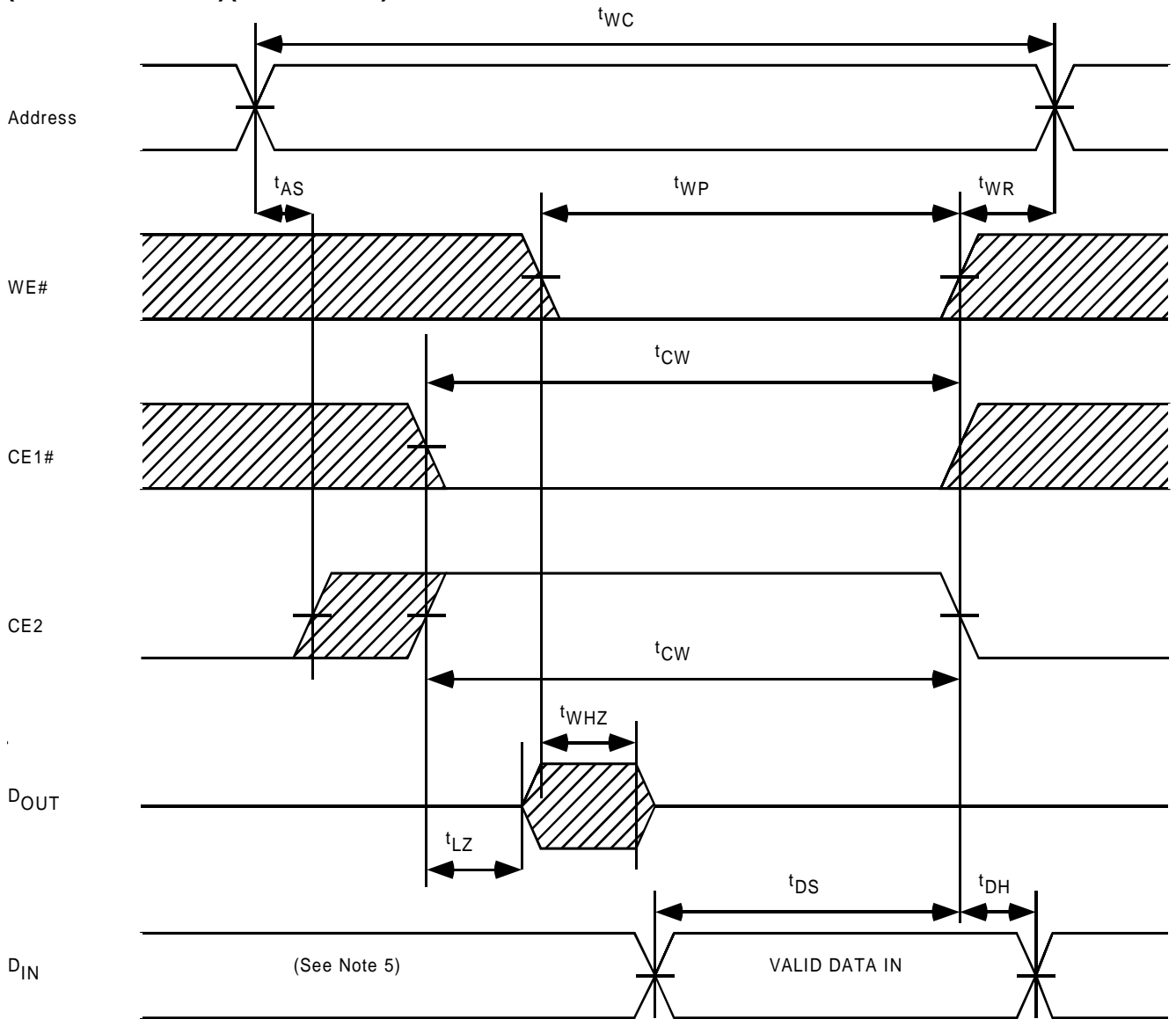
## Write Cycle1 (WE# Controlled)(See Note 4)



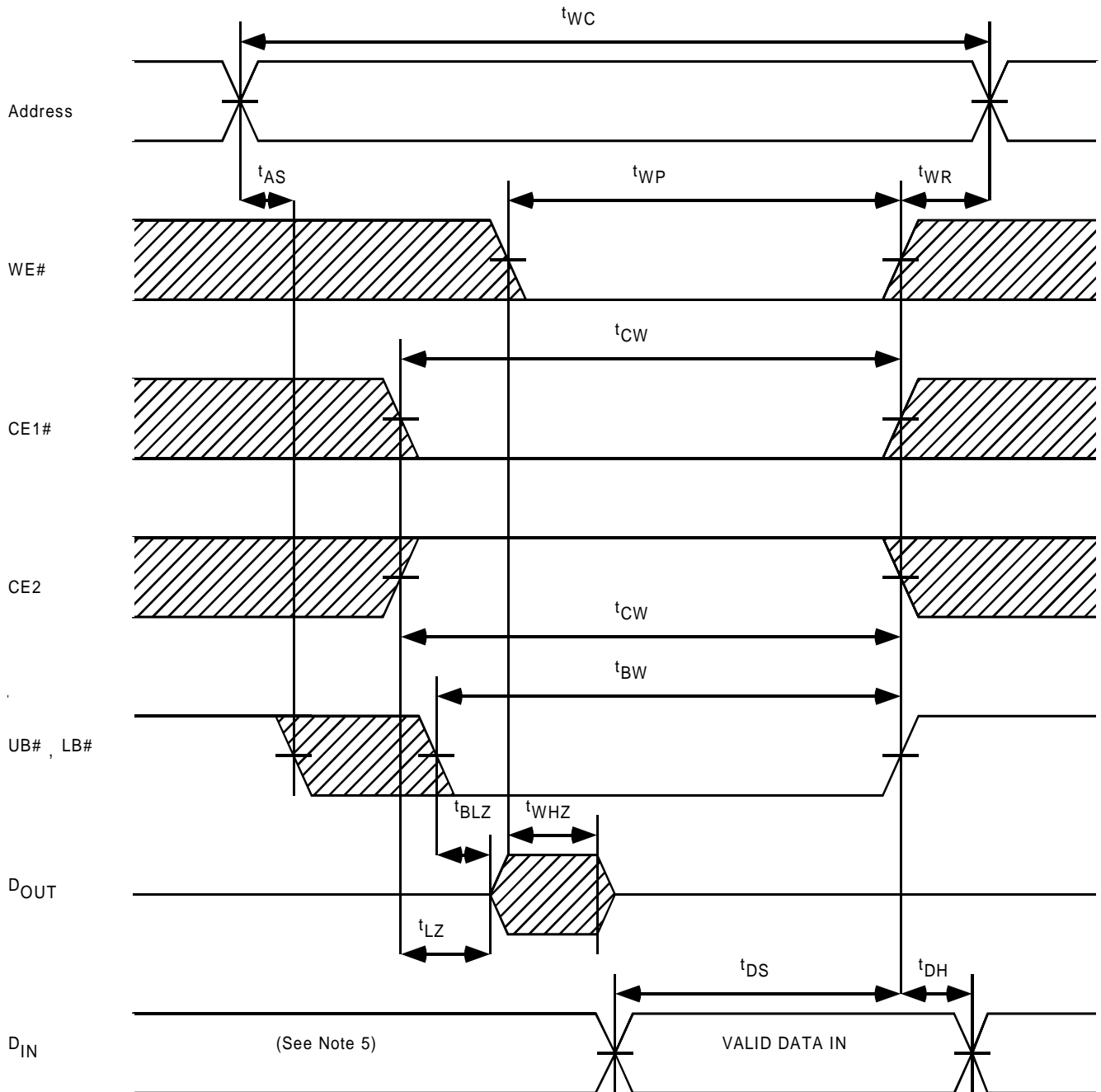
## Write Cycle 2 (CE1# Controlled)(See Note 4)



## Write Cycle 3 (CE2 Controlled)(See Note 4)



## Write Cycle4 (UB#, LB# Controlled)(See Note 4)



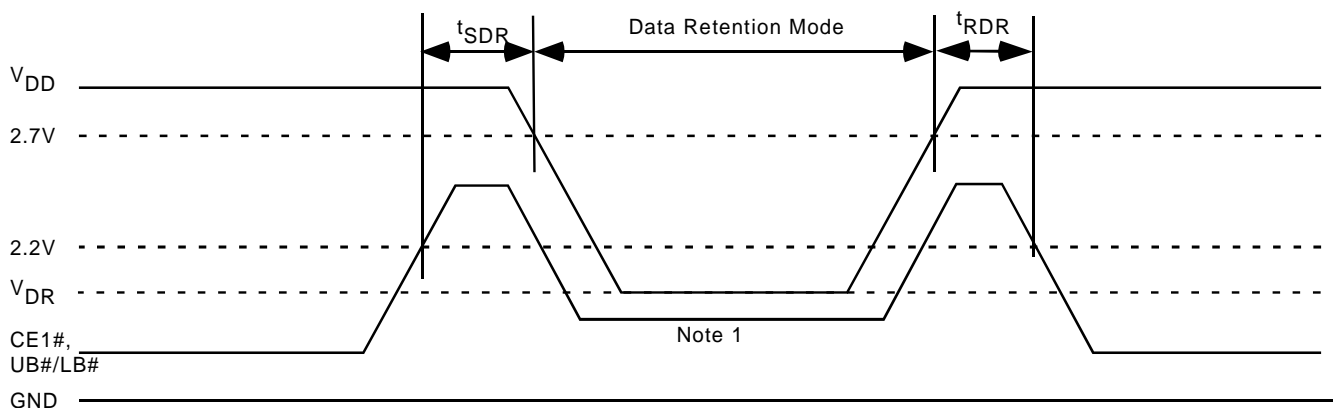
### Note:

1.  $WE\#$  remains HIGH for the read cycle.
2. If  $CE1\#$  goes LOW (or  $CE2$  goes HIGH) with or after  $WE\#$  goes LOW, the outputs will remain at high impedance.
3. If  $CE1\#$  goes HIGH (or  $CE2$  goes LOW) coincident with or before  $WE\#$  goes HIGH, the outputs will remain at high impedance.
4. If  $OE\#$  is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

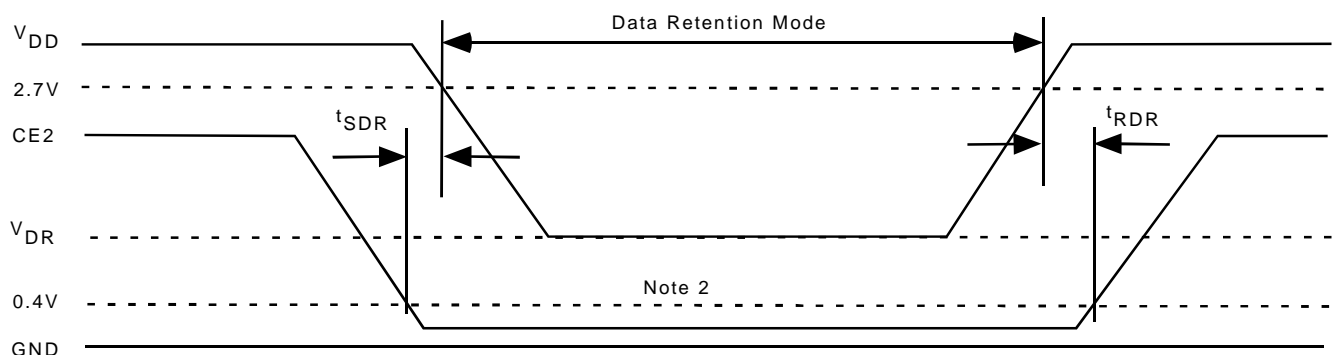
## Data Retention Characteristics (Ta = -40°C to 85°C)

Symbol	Parameter		Min	Typ	Max	Unit
$V_{DR}$	Data Retention Supply Voltage	$CE1\# \geq V_{DD} - 0.2V$ or $UB\# = LB\# \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$ , $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$	1.5	–	3.6	V
$I_{DR}$	Data Retention Current		$V_{DD} = 1.5V, CE\# \geq V_{DD} - 0.2V, V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$		35	$\mu A$
$t_{SDR}$	Chip Deselect to Data Retention Mode Time		0	–	–	ns
$t_{RDR}$	Recovery Time		$t_{RC}$	–	–	ns

### CE1# or UB#/LB# Controlled Data Retention Mode



### CE2 Controlled Data Retention Mode



### Note:

1.  $CE1\# \geq V_{DD} - 0.2V$  or  $UB\# = LB\# \geq V_{DD} - 0.2V$
2.  $CE2 \leq 0.2V$

**Package Diagrams**  
**48-Ball (8mm x 10mm) BGA**  
**Units in mm**

TOP VIEW

BOTTOM VIEW

